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Steve Nishimoto

For: **CIRCUIT AND TECHNIQUE TO STALL THE COMMUNICATION OF DATA OVER A DOUBLE PUMPED BUS**

Enclosed are:

- ☒ Certificate of Mailing with Express Mail Mailing Label No. **EL515090862US**
- ☒ **5** sheets of drawings.
- ☐ A certified copy of a application.
- ☒ Declaration ☒ Signed. ☐ Unsigned.
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Indep. Claims	4	- 3 =	1	x	$78.00	$78.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$690.00
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Dated: 4/03/2000

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INTL-0349-US
(P8539)

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: **CIRCUIT AND TECHNIQUE TO STALL THE COMMUNICATION OF DATA OVER A DOUBLE PUMPED BUS**

APPLICANT: **STEVE NISHIMOTO**

Express Mail No.: EL515090862US
Date: April 3, 2000

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CIRCUIT AND TECHNIQUE TO STALL THE COMMUNICATION OF DATA OVER A DOUBLE PUMPED BUS

BACKGROUND

The invention relates to a circuit and technique to stall the communication of data over a double pumped bus.

As the performance of microprocessors advance, so does the complexity of their designs. As a result of this complexity, more conductive traces, or wires, may be present to route signals across the semiconductor die on which the microprocessor is fabricated. However, it is possible there may be more signals to be routed than there is room in the die to accommodate the corresponding wires.

One solution to this dilemma is to reduce the number of wires that are used to communicate different sets of data. One such arrangement is a double pumped bus, an arrangement in which data is communicated across a single wire in a time multiplexed fashion. Thus, one set of data (that is associated with a particular circuit) is communicated during time slots that are interleaved with other time slots that are used to communicate another set of data (that is associated with another circuit). In this manner, with a double pumped bus, bits from one set of data are communicated to the wire in synchronization with one phase of a clock signal, and bits from another set of data are communicated in synchronization with another phase of the clock signal. For example, one set of data may be communicated across the wire in response to the positive edges (i.e., the rising edges having positive slopes) of a clock signal, and another set of data may be communicated across the wire in response to the negative edges (i.e., the falling edges having negative slopes) of the clock signal.

As a more specific example, Fig. 1 depicts a double pumped bus system 10 to communicate bits of data across a wire 26 between two double pumped bus cells 12 and 14. It is assumed that the cells 12 and 14 share a common ground. As an example, during the logic zero states of a clock signal (called CLK), the cell 12 drives a signal on the wire 26 so that the signal indicates bits of data from a first data set, and during the logic one states of the CLK signal, the cell 12 drives the signal on the wire 26 so that the signal indicates bits of data from a second data set. The cell 14 decodes the bits of data that are indicated by the

signal on the wire 26 and may retransmit the bits of data in a time multiplexed fashion by driving a signal on another wire 27 in a manner similar to that described above. It is noted that, as described below, the cell 14 may be replicated for purposes of forming a larger double pumped system that communicates bits of data over several wires in synchronization with the CLK signal.

As an example, the cell 12 may include a bit latch 16 to latch and temporarily store bits of data from a first set of data and another bit latch 18 to temporarily store bits of data from a second set of data. In this manner, the input terminal of the bit latch 16 may receive a signal (called DATA1) that indicates the bits of the first data set, and the input terminal of the bit latch 18 may receive a signal (called DATA2) that indicates the bits of the second data set. The bit latch 18 is connected to latch bits in response to the positive edges of the CLK signal, and the bit latch 16 is connected to latch bits in response to the negative edges of the CLK signal.

Due to this arrangement, the bit latch 16 responds to each negative edge of the CLK signal by latching the DATA1 signal to store a new bit of the first data set. During the logic zero state of the clock of the CLK signal, the bit latch 16 furnishes a signal (at its non-inverted output terminal) that indicates its stored bit. The bit latch 18 responds to each positive edge of the CLK signal by latching the DATA2 signal to store a new bit of the second data set. During the logic one state of the CLK signal, the bit latch 18 furnishes a signal (at its non-inverted output terminal) that indicates its stored bit.

A multiplexer 20 of the cell 12 selects the output terminals of the bit latches 16 and 18 in response to the above-described logical states of the CLK signal to furnish the bits to the wire 26. As a result, the signal that is furnished by the multiplexer 20 indicates the bits from the first and second data sets in a time multiplexed fashion. It is noted that the cell 14 may have a similar design to the cell 12 except that the input terminals of the bit latches 16 and 18 of the cell 14 are connected together to receive the same signal from the wire 26. Because the bit latch 18 of the cell 14 latches in response to the positive edges of the CLK signal and the bit latch 16 of the cell 14 latches in response to the negative edges of the CLK signal, the bit latches 16 and 18 latch the signal from the wire 26 in alternating time slices to de-multiplex the data. The cell 14 places the bits back into the time multiplexed order for purposes of transmitting the bits across the other wire 27.

Referring to Fig. 2, several cells 12 and 14 (cells 14a, 14b and 14c, as examples) may be serially coupled together to from a chain to relay data between the cells 14 using the double pumped technique that is described above. In this manner, the cell 12 is the first in the chain, and the cells 14 precede the cell 12 in the chain. As an example, Figs. 6, 7 and 8 depict signals called DP1, DP2 and DP3 that are furnished by the cells 12, 14a and 14b, respectively, and illustrate the propagation of data bits between the cells 12 and 14. For example, referring to Figs. 3, 4 and 5, the CLK signal (see Fig. 3) has a negative edge at time T_1, and in response to this negative edge, the cell 12 latches a bit (represented by the portion 50 of the DATA1 signal) for the first data set. At time T_2, the CLK signal has a positive edge, an edge that causes the cell 12 to latch a bit (represented by the portion 50 of the DATA2 signal) for the second data set. After time T_1 during the logic zero state of the CLK signal, the cell 12 begins furnishing the bit 50 to the cell 14a. It is noted that the bit 50 may not appear until after a slight propagation delay, as depicted in Fig. 5. After time T_2 during the logic one state of the CLK signal, the cell 12 begins furnishing the bit 52 to the cell 14a, as depicted in Fig. 6. The cells 14a and 14b then relay the bits 50 and 52 in a time multiplexed fashion as depicted in Figs. 7 and 8.

Unfortunately, the above-described cells only accommodate free flowing data. In this manner, the conventional double pumped bus cell does not have the capability to selectively block the flow of bits from a particular data set.

Thus, there is a continuing need for an arrangement that addresses one or more of the problems that are stated above.

BRIEF DESCRIPTION OF THE DRAWING

Figs. 1 and 2 are schematic diagrams of double pumped bus systems of the prior art.

Figs. 3, 4, 5, 6, 7 and 8 are waveforms illustrating signals of the double pumped bus system of Fig. 2.

Figs. 9 and 11 are schematic diagrams of double pumped bus cells according to embodiments of the invention.

Fig. 10 is a more detailed schematic diagram of the cell of Fig. 9 according to an embodiment of the invention.

Fig. 12 is a schematic diagram of a double pumped bus cell system according to an embodiment of the invention.

Fig. 13 is a schematic diagram of a computer system according to an embodiment of the invention.

DETAILED DESCRIPTION

Referring to Fig. 9, an embodiment 100 of a double pumped bus cell in accordance with the invention may be set up to communicate either one or two sets of data. More specifically, in some embodiments of the invention, an EN signal that is received by the cell 100 may be asserted (driven high, for example) to enable the cell 100 to latch, store and retransmit bits of data from two different data sets in a time multiplexed fashion. In this manner, a data line 107 communicates a signal (called DATAIN) that indicates bits of data from a first data set and a second data set. The bits of the first data set are interleaved, or alternate, in time with the bits of the second data set.

In some embodiments of the invention, when the EN signal is asserted, a bit latch 102 of the cell 100 latches bits one at a time (from the data input line 107) from a first data set in response to the negative edges of a clock signal (called CLK), and another bit latch 104 of the cell 100 latches bits one at a time (also from the data input line 107) from a second data set in response to the positive edges of the CLK signal. The bit latch 102 provides an indication of its latched bit during the logic zero state of the CLK signal, and the bit latch 104 provides an indication of its latched bit during the logic one state of the CLK signal. The select terminal of a multiplexer 106 of the cell 100 receives the CLK signal, selects the output terminal of the bit latch 102 during the logic zero state of the CLK signal and selects the output terminal of the bit latch 104 during the logic one state of the CLK signal. The output terminal of the multiplexer 106 is coupled (via a signal buffer 110) to an output terminal 170 of the cell 100. Thus, due to this arrangement, the cell 100 furnishes the bits of the first and second data sets in a time multiplexed fashion to the output terminal 170 that may be coupled to a double pumped bus wire, for example.

It is noted that, at least in some embodiments of the invention, the cell 100 receives bits from the first data set during the logic one states of the CLK signal, latches these bits in response to the negative edges of the CLK signal and furnishes these bits to the output

terminal 170 during the logic zero states of the CLK signal. The cell 100 receives bits from the second data set during the logic zero states of the CLK signal, latches these bits in response to the positive edges of the CLK signal and furnishes these bits to the output terminal 170 during the logic one states of the CLK signal. Thus, the cell 100 reverses the phases between the incoming and outgoing data streams.

It is possible that in a particular scenario, it may not be desirable to communicate both sets of data through the cell 100. For example, in some embodiments, the EN signal may be de-asserted (driven low, for example) to disable the bit latch 104 from latching new bits of data (from the second data set) from the data input line 107. Thus, by disabling the bit latch's ability to receive bit updates, the flow of the second set of data may be effectively halted through the cell 100.

Thus, the double pumped cell 100 may be used in at least two ways. In a chain of double pumped cells, the EN signal may be asserted in each of the cells to enable the communication of both sets of data through the chain. As described above, in some embodiments of the invention, the operation of the bit latch 102 is not affected by the EN signal, as the bit latch 102 responds to the CLK signal, regardless of the state of the EN signal. When the EN signal is asserted for a particular cell 100, both sets of data propagate though the bit latches 102 and 104. Thus, as an example, a particular bit propagates through the bit latch 102 of one cell in the chain, propagates through the bit latch 104 of the next cell in the chain, propagates through the bit latch 102 of the next cell in the chain, etc. The double pumped cell 100 may also be used in the chain to filter out the communication of one of the sets of data through the chain. For this arrangement, the EN signal is deasserted in every other cell to alternate which bit latch 102, 104 is disabled, as bits of a particular data set alternate between the bit latches 102 and 104 as the data propagates through the chain.

To accomplish the above-described features, in some embodiments of the invention, the cell 100 may include logic, such as an AND gate 112, that receives the CLK and EN signals. The output terminal of the AND gate 112 is coupled to the inverting clock input terminal of the bit latch 104, and the clock input terminal of the bit latch 106 receives the CLK signal. Because the bit latches 102 and 104, in some embodiments of the invention, invert the logic levels of the stored bits, the cell 100 may include an inverter 108 that is coupled between the data input line 107 and the input terminals of the bit latches 102 and

104. When the EN signal is de-asserted, the output terminal of the AND gate 112 is de-asserted, regardless of the logic level of the CLK signal, and thus, the bit latch 104 does not store any new data as long as the EN signal remains de-asserted. However, when the EN signal is asserted, the CLK signal controls the signal at the output terminal of the AND gate 112 and thus, controls the reception of data into the bit latch 104.

Fig. 10 depicts a more detailed schematic diagram of the cell 100 in accordance with some embodiments of the invention. As shown, the bit latch 102 may include a circuit 140 that is effectively a complementary metal oxide semiconductor (CMOS) inverter that is enabled when the CLK signal (that alternates between logic one and logic zero states) is in a logic one state to latch the bit that is indicated by the DATAIN signal. To accomplish this, the circuit 140 includes an n-channel metal-oxide-semiconductor field-effect-transistor (NMOSFET) 148 that has its source terminal coupled to ground and its drain terminal coupled to the source terminal of another NMOSFET 146. The drain terminal of the NMOSFET 146 is coupled to the drain terminal of a p-channel metal-oxide-semiconductor field-effect-transistor (PMOSFET) 144. The source terminal of the PMOSFET 144 is coupled to the drain terminal of another PMOSFET 142, and the drain terminal of the PMOSFET 142 is coupled to a positive voltage supply level (called V_{DD}). The gate terminals of the PMOSFET 144 and the NMOSFET 146 respond to the logical state of the CLK signal to control when the circuit 140 is enabled. In this manner, the gate terminal of the PMOSFET 144 is coupled to a clock input terminal 131 (that furnishes the CLK signal) via a chain 124 of three serially coupled inverters 240 that invert the CLK signal to receive an inverted version of the CLK signal. The gate terminal of the NMOSFET 146 is coupled to a chain 123 of serially coupled inverters 120 to the clock line 131 to receive an indication of the CLK signal. The gate terminals of the PMOSFET 144 and the NMOSFET 148 are coupled to the data input line 107.

For purposes of storing the bit inside the bit latch 102, the buffer 102 includes a latch circuit that is formed by two inverters 160 and 162 that are coupled together in a back-to-back arrangement. The input terminal of the inverter 160 and the output terminal of the inverter 162 are coupled together to the drain terminal of the NMOSFET 146. An inverter 164 is coupled between the drain terminal of the NMOSFET 146 and the multiplexer 106. Thus due to this arrangement, when the circuit 140 is enabled during the logic one state of the

CLK signal, the CMOS inverter (formed by the transistors 142, 144, 146 and 148) drives the inverters 160 and 162 to update the state of the stored bit, and when the CLK signal transitions from the logic one to the logic zero state on a negative edge, the CMOS inverter becomes disabled to latch the bit that is stored in the inverters 160 and 162.

Similar to the bit latch 102, the bit latch 104 includes the circuit 140 and the bit latch that is formed from inverters 160 and 162. However, unlike the bit latch 102, the gate terminals of the circuit 140 of the bit latch 140 are connected differently. In this manner, the gate terminal of the PMOSFET 144 is coupled to the output terminal of a NAND gate 124, and the gate terminal of the NMOSFET 146 is coupled to the output terminal of an inverter 136 that has its input terminal coupled to the output terminal of the NAND gate 124. One input terminal of the NAND gate 124 is coupled between the inverter 120 to receive an inverted indication of the CLK signal, and the other input terminal of the NAND gate 124 is coupled to an enable input line 113 to receive the EN signal. Thus, when the EN signal is asserted, the circuit 140 of the bit latch 104 is enabled during the logic zero state of the CLK signal to update the bit that is stored by the inverters 166 and 168 of the circuit 140. During the logic one state of the CLK signal and when the EN signal is de-asserted, the circuit 140 is disabled. Thus, when the CLK signal transitions from the logic zero to the logic one state on a positive edge, the CMOS inverter becomes disabled to latch the bit that is stored in the inverters 160 and 162 of the bit latch 104.

In some embodiments of the invention, the multiplexer 106 includes two CMOS pass gates 172 and 174. The input terminal of the CMOS pass gate 172 is coupled to the output terminal of the inverter 164 of the bit latch 102, and the output terminal of the CMOS pass gate 172 is coupled to a node 168 that forms the output terminal of the multiplexer 106. The inverting control, or selection, terminal of the pass gate 172 is coupled to the gate terminal of the NMOSFET 146 of the bit latch 102, and the non-inverting control, or selection, terminal of the pass gate 172 is coupled to the gate terminal of the PMOSFET 144 of the bit latch 102. Thus, due to this arrangement, the output terminal of the bit latch 102 is coupled to the output terminal of the multiplexer 160 when the CLK signal has a logic zero level. The input terminal of the CMOS pass gate 174 is coupled to the output terminal of the inverter 164 of the bit latch 104, and the output terminal of the CMOS pass gate 174 is coupled to the node 168. The inverting control terminal of the pass gate 174 is coupled to the non-inverting

control terminal of the pass gate 172, and the non-inverting control terminal of the pass gate 174 is coupled to the inverting control terminal of the pass gate 172. Thus, due to this arrangement, the output terminal of the bit latch 104 is coupled to the output terminal of the multiplexer 160 when the CLK signal has a logic one level. In some embodiments of the invention, the inverter 110 may include a chain of three inverters 109 that are coupled between the node 168 and the output terminal 170.

The cell 100 that is described above receives time-multiplexed bits of data from a single wire. However, in some embodiments of the invention, a cell 200 that is depicted in Fig. 11 may be used in place of the cell 100. The cell 200 has a similar design to the cell 100 except for the following features. Unlike the cell 100, the cell 200 has two data input lines 203 and 205 (instead of one) to receive bits of data from circuits that are associated with two different data sets. In this manner, the inverter 108 (see Fig. 9) of the cell 100 is replaced by two inverters 202 and 207 of the circuit 200. The input terminal of the inverter 202 receives a signal (called DATA1) that is indicative of bits of data from the first data set, and the input terminal of the inverter 207 receives a signal (called DATA2) that is indicative of bits of data from the second data set. The output terminal of the inverter 202 is coupled to the data input line of the bit latch 102, and the output terminal of the inverter 207 is coupled to the data input line of the bit latch 104.

Referring to Fig. 12, in some embodiments of the invention, the cells 100 (the enabled cells 100a and the disabled cells 100b, as described below) and 200 may be used to form a double pumped bus chain 220 for purposes of communicating the bits of data from the first and second data sets across an integrated circuit, for example. In this manner, the cell 200 is the first in the chain 220 to arrange bits from the two different data sets in a time interleaved fashion. The cells 100 may be serially coupled together after the cell 200. As shown, to disable the flow of the bits of the data set that is associated with the DATA2 signal, every other cell 100 is disabled, as depicted in Fig. 12 by the enabled cells 100a and the disabled cells 100b. This alternative disabling of the cells 100 occurs because each cell 100 reverses the phasing of the data flow. For example, each cell 100 receives the bits of a particular data set on positive clock edges and retransmits the bits of that data set on negative clock edges. The arrangement that is depicted in Fig. 12 is used to disable the flow of bits for the data set that is associated with the DATA2 signal. However, alternatively, to disable the bits for the

data set that is associated with the DATA1 signal, the enable input terminals 113 of the cells 200 and 100b are asserted, and the enable input terminals 113 of the cells 100a are de-asserted.

Referring to Fig. 13, as an example, the cell 200 (and/or the cell 100) may be used in a semiconductor circuit, such as a processor 252 (a microprocessor, such as a Pentium® microprocessor, as an example), to communicate bits of data between circuits 254, 256, 260 and 262 of the processor 252. In this manner, the cell 200 may communicate data over a wire 258 for two data sets. More specifically, the cell 200 may communicate data for a first data set between the circuit 254 that is located at one end of the wire 258 and the circuit 260 that is located at another end of the wire 268. The cell 200 may also communicate data for a second data set between the circuit 256 that is located at one end of the wire 258 and the circuit 262 that is located at the other end of the wire 268.

Among the other components of the computer system 250, the computer system 250 may include a local bus 270 that is coupled to the processor 252 and is also coupled to a north bridge, or memory hub 272. As an example, the memory hub 272 may provide interfaces for a Peripheral Component Interface (PCI) bus 284, an Accelerated Graphics Port (AGP) bus 286 and a memory bus 276. The AGP is described in detail in the Accelerated Graphics Port Interface Specification, Revision 1.0, published on July 31, 1996, by Intel Corporation of Santa Clara, California. The PCI Specification is available from The PCI Special Interest Group, Portland, Oregon 97214. The memory bus 276 communicates data between the memory hub 272 and a system memory 274. A display controller 287 may be coupled the AGP bus 286 and drive a display 289. A hub bus 289 may establish communication between the memory hub 272 and a south bridge, or input/output (I/O) hub 290.

The I/O hub 290 may, for example, control operation of a CD-ROM drive 292 and a hard disk drive 294. The I/O hub 290 may also provide an interface to an I/O expansion bus 296. An I/O controller 298 may be coupled to the I/O expansion bus 296. The I/O controller 298 may, for example, receive input data from a mouse 300 and a keyboard 302 and control operation of a floppy disk drive 304. The computer system 250 is one out of many different embodiments, all of which are within the scope of the appended claims.

While the invention has been disclosed with respect to a limited number of embodiments, those skilled in the art, having the benefit of this disclosure, will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of the invention.

What is claimed is:

1. An apparatus comprising:

a first circuit to receive indications of first data associated with a first data set and second data associated with a second data set; and

a second circuit coupled to the first circuit to cause the first circuit to:

in a first mode, communicate indications of the first data to an output terminal in synchronization with a first phase of a clock signal and communicate indications of the second data to the output terminal in synchronization with a second phase of the clock signal, and

in a second mode, communicate the indications of the first data to the output terminal in synchronization with the first phase and prevent communication of the second data during the second phase.

2. The apparatus of claim 1, wherein the first circuit comprises:

a first latch to store at least one bit at a time of the first data; and

a second latch to, at least in the first mode, store at least one bit at a time of the second data.

3. The apparatus of claim 2, wherein the first latch transfers said at least one bit of the first data in response to a predefined edge of the clock signal.

4. The apparatus of claim 2, wherein, in the first mode, the second latch transfers said at least one bit of the second data in response to a predefined edge of the clock signal.

5. The apparatus of claim 4, further comprising:

logic to selectively provide the clock signal to the second latch based on whether the apparatus is in the first or second mode.

6. The apparatus of claim 5, wherein the logic does not provide the clock signal to the second latch in the second mode.

7. The apparatus of claim 5, wherein the logic comprises:

an AND gate including a first input terminal to receive a mode select signal, a second input terminal to receive the clock signal and an output terminal coupled to a clock input terminal of the second latch.

8. The apparatus of claim 2, further comprising:

a multiplexer including an output terminal that is coupled to the output terminal of the apparatus, the multiplexer alternatively selecting the first and second latch in response to the first and second phases of the clock signal.

9. The apparatus of claim 1, wherein the apparatus comprises a double pumped bus circuit.

10. A computer system comprising:

a system memory; and

a processor coupled to system memory, the processor including:

a wire;

a first circuit to receive indications of first data associated with a first data set and second data associated with a second data set; and

a second circuit coupled to the first circuit to cause the first circuit to:

in a first mode, communicate indications of the first data to the wire synchronization with a first phase of a clock signal and communicate indications of the second data to the wire in synchronization with a second phase of the clock signal, and

in a second mode, communicate the indications of the first data to the wire in synchronization with the first phase and prevent communication of the second data during the second phase.

11. The computer system of claim 10, wherein the first circuit comprises:

a first latch to store at least one bit at a time of the first data; and

a second latch to, at least in the first mode, store at least one bit at a time of the second data.

12. The computer system of claim 11, wherein the first latch transfers said at least one bit of the first data in response to a predefined edge of the clock signal.

13. The computer system of claim 11, wherein, in the first mode, the second latch transfers said at least one bit of the second data in response to a predefined edge of the clock signal.

14. The computer system of claim 13, further comprising:

logic to selectively provide the clock signal to the second latch based on whether the apparatus is in the first or second mode.

15. A system comprising:

double pumped bus circuits serially coupled together to form a chain to communicate data from at least two different sets of data, at least one of the bus circuits being capable of being disabled to prevent bits from at least one of the sets of data from being communicated through said at least one of the bus circuits.

16. The system of claim 15, wherein alternate double pumped circuits are disabled to prevent the bits from at least one of the sets of data form being communicated through said at least one of the bus circuits.

17. The system of claim 15, wherein each double pumped circuit latches bits from one of the sets of data in response to first edges of a clock signal and furnishes indications of the bits in response to second edges of the clock signal, the first edges being different from the second edges.

18. The system of claim 17, wherein the first edges comprises positive edges of the clock signal.

19. The system of claim 17, wherein the first edges comprises negative edges of the clock signal.

20. A method comprising:

receiving first indications of first data associated with a first data set;

receiving second indications of second data associated with a second data set;

in a first mode, communicating the first indications to a double pumped bus in synchronization with a first phase of a clock signal and communicating the second indications to the double pumped bus in synchronization with a second phase of the clock signal; and

in a second mode, communicating the first indications to the double pumped bus in synchronization with the first phase and preventing communication of the second indications to the double pumped bus during the second phase.

21. The method of claim 20, wherein the receiving the first indications comprises:

latching the first indications one bit at a time.

22. The method of claim 20, wherein the receiving the second indications comprises:

latching the second indications one bit at a time.

23. The method of claim 20, wherein the communicating during the first mode comprises:

communicating bits of the first data in response to first predefined edges of the clock signal; and

communicating a bits of the second data in response to other predefined edges of the clock signal, said other predefined edges being different from the first predefined clock edges.

CIRCUIT AND TECHNIQUE TO STALL THE COMMUNICATION OF DATA OVER A DOUBLE PUMPED BUS

ABSTRACT OF THE DISCLOSURE

An apparatus includes a first circuit and a second circuit. The first circuit receives indications of first data that is associated with a first data set and second data that is associated with a second data set. The second circuit is coupled to the first circuit to cause the first circuit to in a first mode, communicate indications of the first data to an output terminal in synchronization with a first phase of a clock signal and communicate indications of the second data to the output terminal in synchronization with a second phase of the clock signal. In a second mode, the second circuit causes the first circuit to communicate the indications of the first data to the output terminal in synchronization with the first phase and prevent communication of the second data during the second phase.

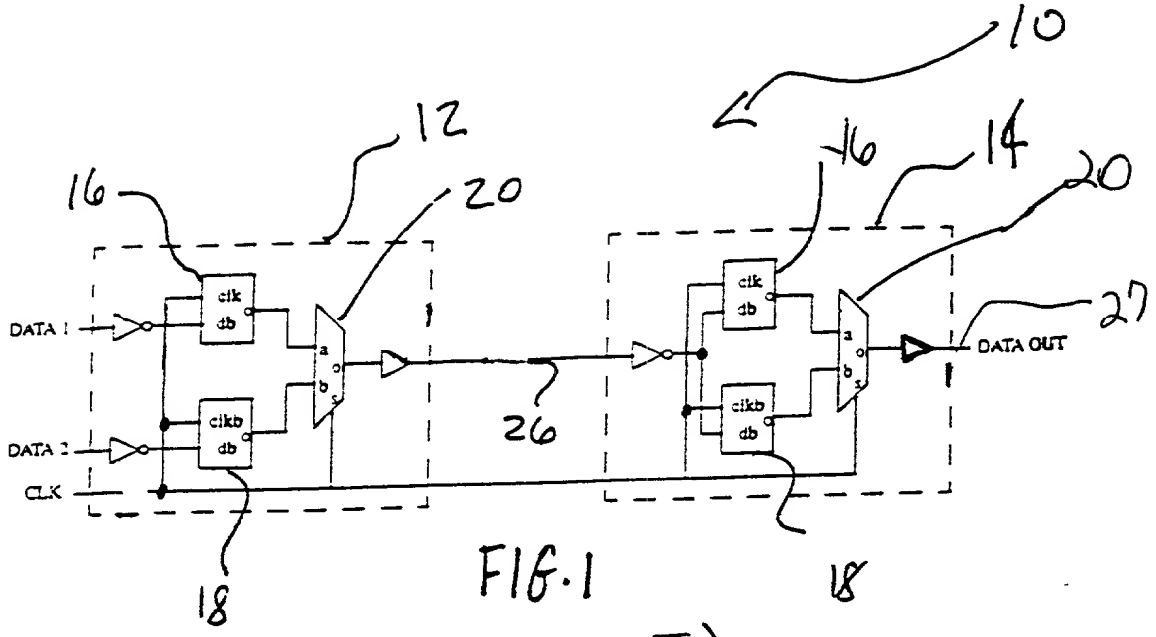

FIG. 1
(PRIOR ART)

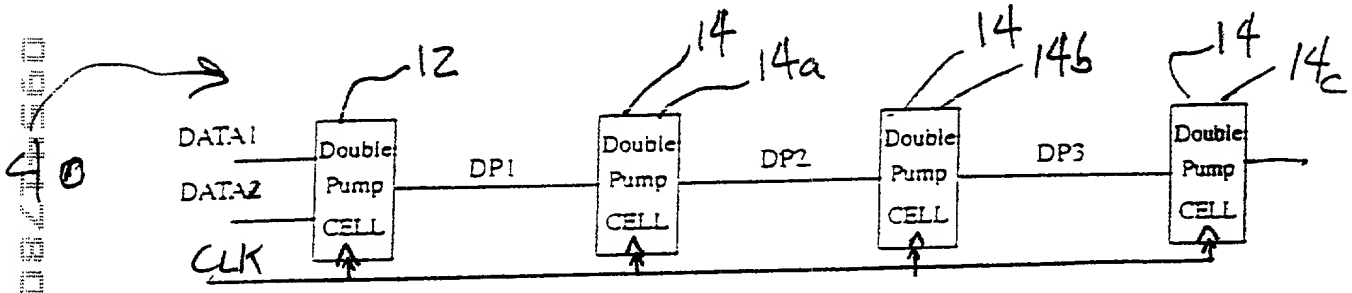

FIG. 2
(PRIOR ART)

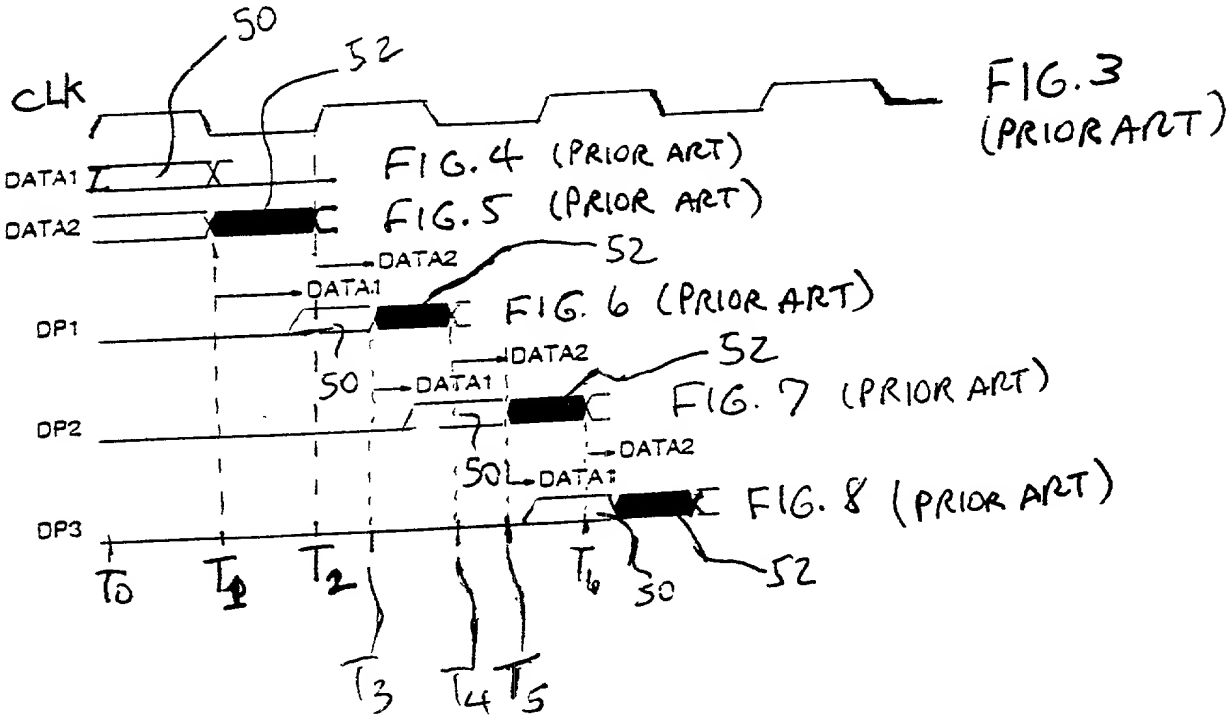

FIG. 3
(PRIOR ART)

FIG. 4 (PRIOR ART)

FIG. 5 (PRIOR ART)

FIG. 6 (PRIOR ART)

FIG. 7 (PRIOR ART)

FIG. 8 (PRIOR ART)

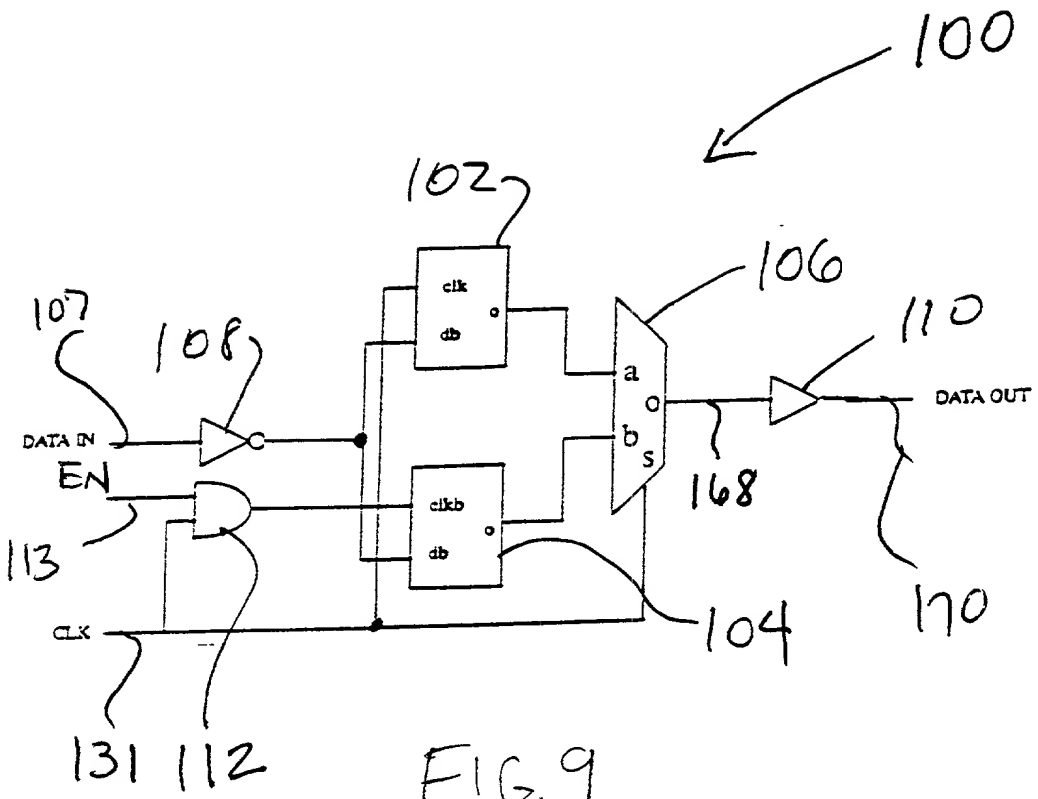
100
102
clk
db
106
107
108
110
DATA IN
EN
a
o
b
s
DATA OUT
168
clkb
db
113
CLK
104
170
131
112

FIG. 9

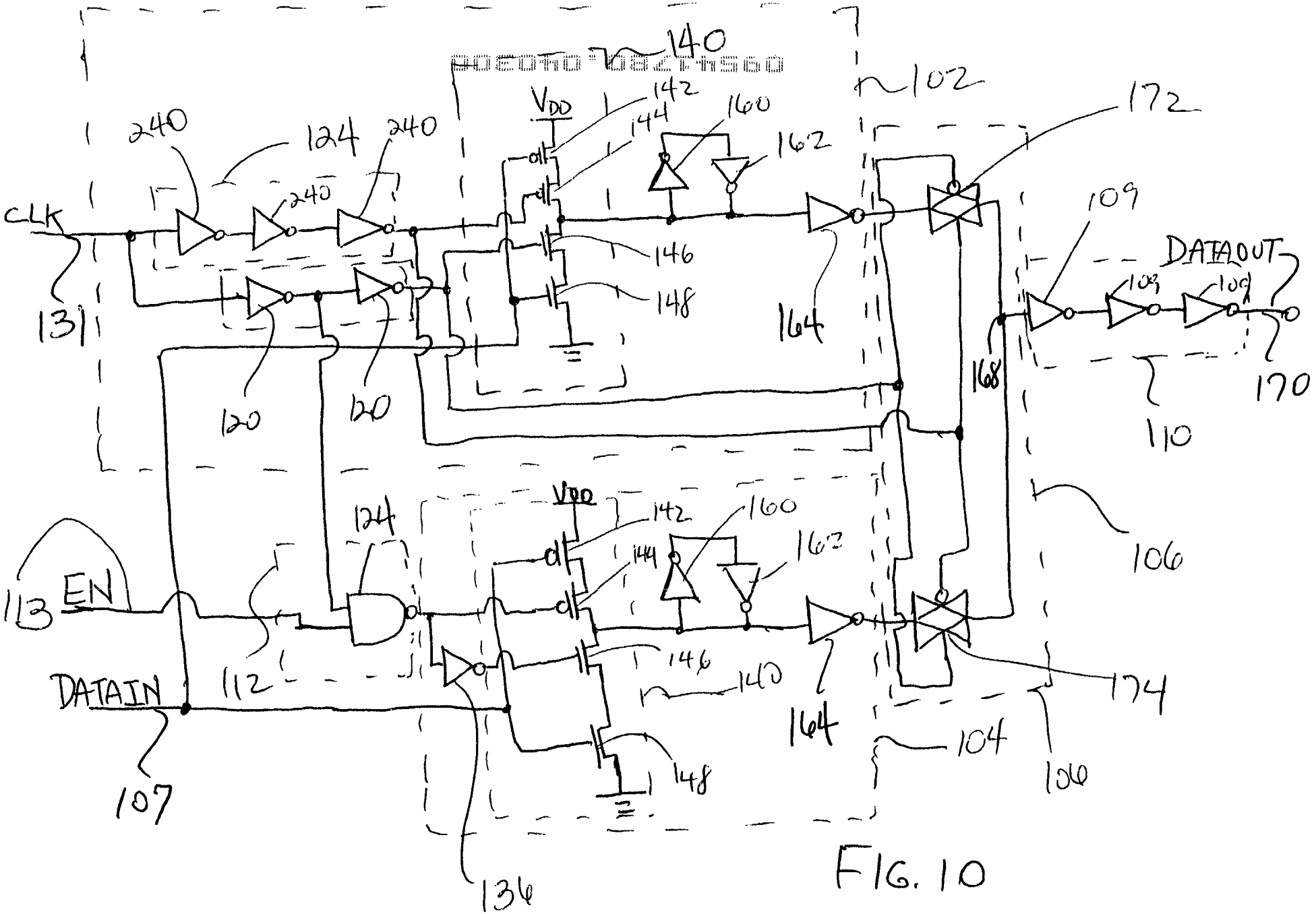
140
102
172
240
124
240
240
V_{DD}
142
144
160
162
CLK
109
DATAOUT
146
148
164
131
120
120
168
103
105
110
170
106
V_{DD}
142
160
124
144
162
113
EN
146
140
DATAIN
112
164
174
104
107
106
148
136

FIG. 10

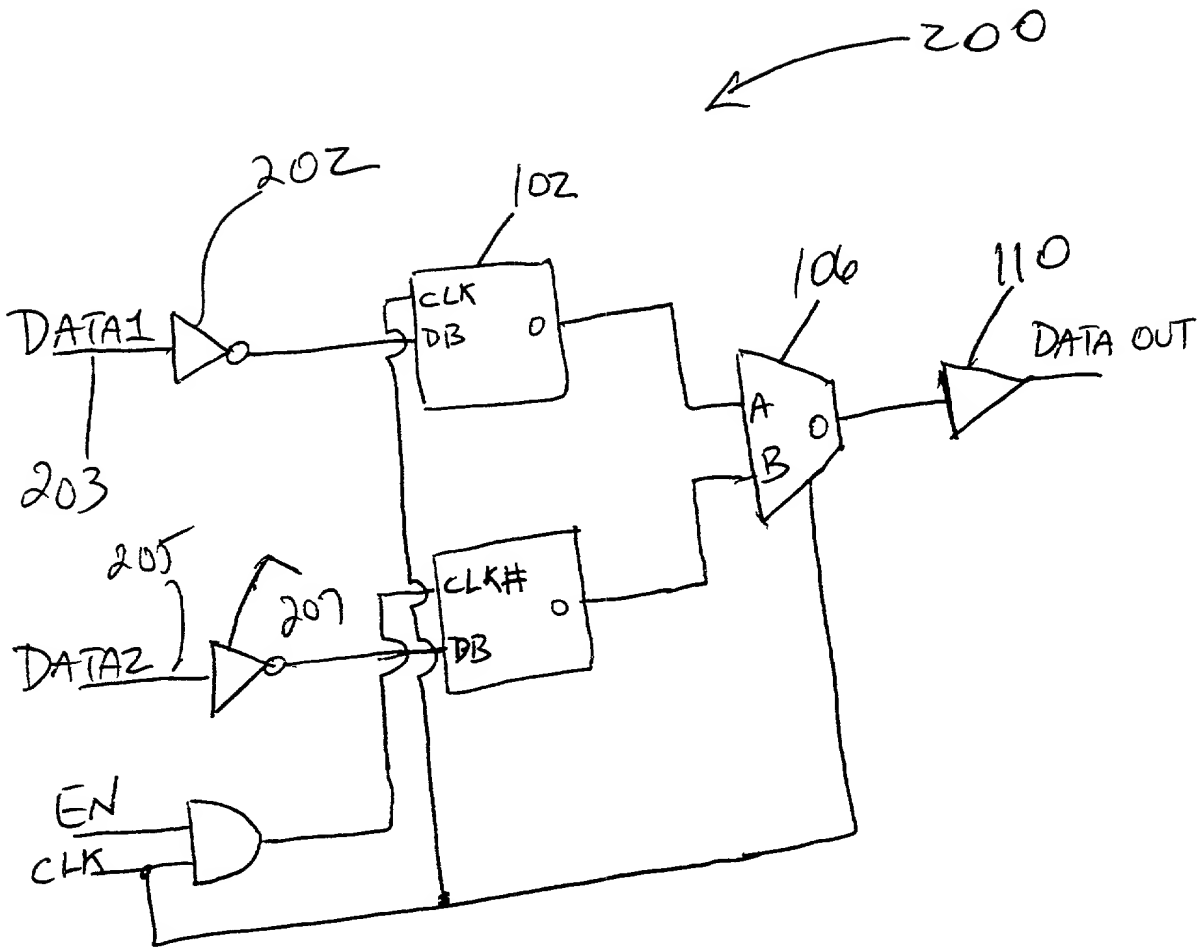
200
202
102
106
110
DATA1
203
CLK
DB
O
A
B
O
DATA OUT
205
207
DATA2
CLK#
O
DB
EN
CLK

FIG. 11

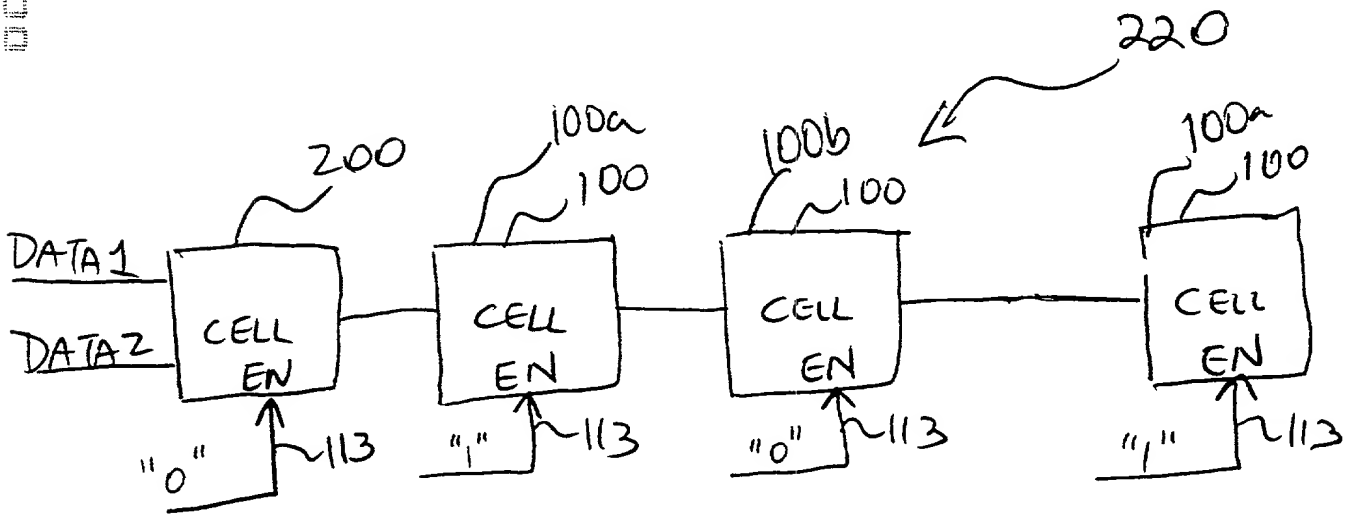
220
200
100a
100
100b
100
100a
100
DATA1
DATA2
CELL
EN
CELL
EN
CELL
EN
CELL
EN
"0"
113
"1"
113
"0"
113
"1"
113

FIG. 12

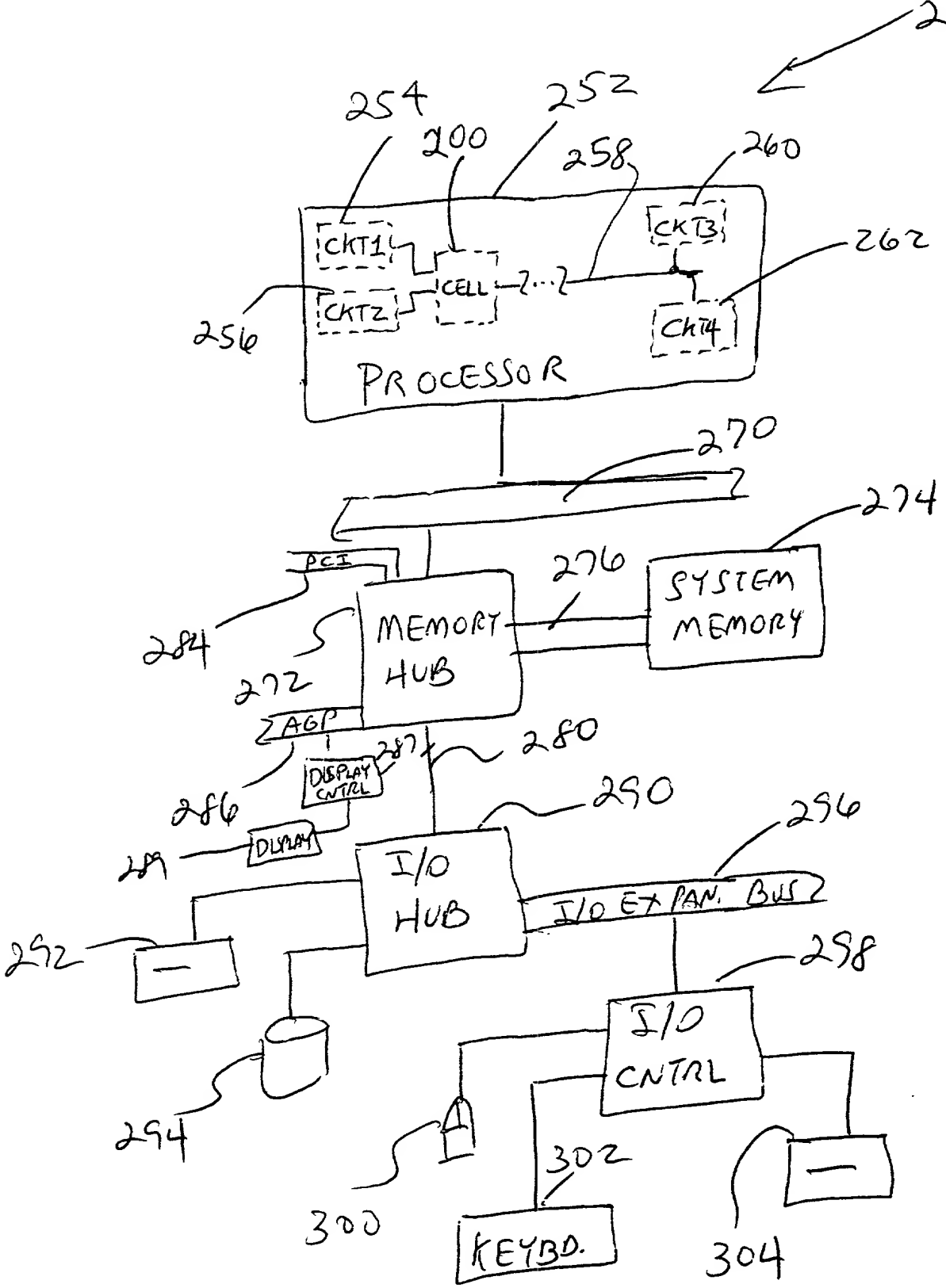
250
254
252
200
258
260
CKT1
CKT3
262
CELL
CKT2
CKT4
256
PROCESSOR
270
274
PCI
276
SYSTEM MEMORY
284
MEMORY HUB
272
AGP
280
287
DISPLAY CNTRL
286
290
256
DISPLAY
289
I/O HUB
I/O EXPAN. BUS
292
298
I/O CNTRL
294
302
300
KEYBD.
304

FIG. 13

Attorney's Docket No.: INTL-0349 -US (P8539) PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

CIRCUIT AND TECHNIQUE TO STALL THE COMMUNICATION OF DATA OVER A DOUBLE PUMPED BUS

the specification of which

X	is attached hereto.
	was filed on _____ as
	United States Application Number _____
	or PCT International Application Number _____
	and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate Issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):			Priority Claimed	
Number	(Country)	(Day/Month/Year Filed)	Yes	No
Number	(Country)	(Day/Month/Year Filed)	Yes	No

Number	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of the United States provisional application(s) listed below:

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Number)	Filing Date	(Status-patented, pending, abandoned)
(Application Number)	Filing Date	(Status-patented, pending, abandoned)

I hereby appoint Timothy N. Trop, Reg. No. 28,994; Fred G. Pruner, Jr., Reg. No. 40,779 and Dan C. Hu, Reg. No. 40,025 my patent attorneys, of TROP, PRUNER & HU, P.C., with offices located at 8554 Katy Freeway, Ste. 100, Houston, TX 77024, telephone (713) 468-8880, and Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Sean Fitzgerald, Reg. No. 32,027; David J. Kaplan, Reg. No. 41,105; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; and Charles K. Young, Reg. No. 39,425; my patent attorneys, of INTEL CORPORATION; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Timothy N. Trop, TROP, PRUNER & HU, P.C., 8554 Katy Freeway, Ste. 100, Houston, TX 77024 and direct telephone calls to Fred G. Pruner, Jr. (713) 468-8880.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor: **STEVE NISHIMOTO**	
Inventor's Signature: Steve Nishimoto	Date: 3/31/00
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Post Office Address: **1 DUANE ST. #34, REDWOOD CITY, CA 94062**	